CLAIMS

1. A method for re-using diffused cell-based IP blocks in a structured application specific integrated circuit comprising the steps of:

implementing one or more blocks of intellectual property (IP) using a plurality of cell-based building blocks; and

providing one or more alternative views for at least one of said one or more blocks of intellectual property.

2. The method according to claim 1, wherein said cell-based building blocks comprise one or more standard cell gates.

3. The method according to claim 1, wherein said cell-based building blocks comprise one or more of a logic gate, a buffer and a flip-flop.

4. The method according to claim 2, wherein placement of said standard cell gates is fixed when said one or more blocks of intellectual proper are placed on a base wafer.

5. The method according to claim 1, further comprising the step of:

generating said one or more alternative views during design of said one or more blocks of intellectual property.

6. The method according to claim 5, wherein one or more of said alternative views are generated manually.

7. The method according to claim 5, wherein one or more of said alternative views are generated with a text editor.

8. The method according to claim 5, wherein said one or more alternative views are generated automatically.

9. The method according to claim 8, wherein said one or more alternative views are generated from RTL using ECO compiler tools that target an existing set of diffused cell-based gates.

10. The method according to claim 5, wherein one or more of said alternative views are generated prior to instantiation.

11. The method according to claim 1, wherein generating said one or more alternative views comprises the step of:

modifying a netlist for each of said one or more blocks of intellectual property.

12. The method according to claim 11, wherein any unused building blocks are tied off in said modified netlist.

13. The method according to claim 11, further comprising the step of:

mapping said modified netlist onto a placement of a corresponding one of said one or more blocks of intellectual property.

14. The method according to claim 13, further comprising the step of:

generating a layout view of said one or more blocks of intellectual property corresponding to said modified netlist.

15. The method according to claim 14, further comprising the step of:

routing said one or more blocks of intellectual property based upon said modified netlist.

16. A computer readable medium comprising:

a default view of one or more blocks of intellectual property; and

one or more alternative views of at least one of said one or more blocks of intellectual property.

17. The computer readable medium according to claim 16, wherein said one or more alternative views comprise a modified netlist for said at least one of said one or more blocks of intellectual property.

18. an integrated circuit comprising:

a base layer containing one or more blocks of intellectual property (IP) using a plurality of cell-based building blocks; and

one or more metal layers instantiating said one or more blocks of intellectual property, wherein said one or more metal

layers comprise routing based upon an alternative view for at least one of said one or more blocks of intellectual property.

19. The integrated circuit according to claim 18, wherein said alternative view comprises a modified netlist for said at least one block of intellectual property.

20. The integrated circuit according to claim 19, wherein said modified netlist for said at least one block of intellectual property comprises one or more standard cell gates that are tied off.